CLAIMS:

1. A wafer (1), which wafer (1) comprises a number of exposure fields (2) and which wafer (1) comprises a number of intersecting, lattice-like dicing path sections (6A, 6B, 6C, 8A, 8B, 8C, 8D) and a number of lattice fields (3) in each exposure field (2), wherein each lattice field (3) contains an IC (4), and which wafer (1) comprises a first group (5) of first dicing paths (6) and a second group (7) of second dicing paths (8), wherein all of the first dicing paths (6) of the first group (5) run parallel to a first direction (X) and have a first path width (W1) and wherein all of the second dicing paths (8) of the second group (7) run parallel to a second direction (Y) intersecting the first direction (X) and have a second path width (W2), and wherein the first dicing paths (6) consist of a plurality of first dicing path sections (6A, 6B, 6C) arranged consecutive to one another in the first direction (X) and the second dicing paths (8) consist of a plurality of second dicing path sections (8A, 8B, 8C, 8D) arranged consecutive to one another in the second direction (Y), and wherein the first dicing paths (6) and the second dicing paths (8) are provided and designed for a subsequent segregation of the lattice fields (3) and the ICs (4) contained therein, and wherein each exposure field (2) has a first edge (R1, S1, T1) extending parallel to the first direction (X) and a second edge (R2, S2, T1) extending parallel to the first direction (X) and lying opposite the first edge (R1, S1, T1), and wherein at least two control module fields (A1, A2, B1, B2, C1, D1, D2, E1, E2, F1) are assigned to each exposure field (2), each of which control module fields contains at least one optical control module (OCM-A1, OCM-A2, OCM-B1, OCM-B2, OCM-C1, OCM-D1, OCM-D2, OCM-E1, OCM-E2, OCM-F1), and wherein a first control module field (OCM-A1, OCM-B1, OCM-C1, OCM-D1, OCM-E1, OCM-F1) of each exposure field (2) immediately adjoins the first edge (R1, S1, T1) of the exposure field (2) in question and lies between the first edge (R1, S1, T1) and a row of lattice fields (3) extending parallel to the first direction (X) in a first dicing path section (6A, 6B, 6C) and thus in a first dicing path (6), and wherein a second control module field (OCM-A2, OCM-B2, OCM-D2, OCM-E2) of each exposure field (2) lies at a preset distance from the second edge (R2, S2) between two rows of lattice fields (3) extending parallel to the first direction (X) and arranged adjacent to one another, and thus likewise in a first dicing path (6).

2. A wafer (1) as claimed in claim 1, wherein the second control module field (OCM-A2, OCM-B2, OCM-D2, OCM-E2) of each exposure field (2) immediately adjoins the row of lattice fields (3), which row of lattice fields (3) immediately adjoins the second edge (R2, S2) of the exposure field (2) in question.